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<b>(21) International Application Number:</b> PCT/GB99/03897 <b>(22) International Filing Date:</b> 24 November 1999 (24.11.99) <b>(30) Priority Data:</b> 9826592.9      4 December 1998 (04.12.98)      GB <b>(71) Applicant (for all designated States except US):</b> SYSTOLIX LIMITED [-/GB]; 4th floor, India Buildings, Water Street, Liverpool L2 0QT (GB). <b>(72) Inventor; and</b> <b>(75) Inventor/Applicant (for US only):</b> DEWHURST, Andrew [GB/GB]; 3 Bramble Close, Gentrys Green, Middlewich, Cheshire CW10 9FZ (GB). <b>(74) Agent:</b> EVERY, David, Aidan; Marks & Clerk, Sussex House, 83-85 Mosley Street, Manchester M2 3LG (GB).		<b>(81) Designated States:</b> AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).  <b>Published</b> <i>With international search report.</i>

**(54) Title:** A SERIAL-PARALLEL BINARY MULTIPLIER**(57) Abstract**

A serial binary multiplier multiplies two operands to provide a product. A first operand is stored locally and a second operand is transmitted serially whilst simultaneously multiplying said first operand with all possible values of said second operand taking into account any received bits of the second operand. All possible results are added to the contents of a partial result register and stored and when a complete element of the full second operand has been received and decoded, the correct result is selected by the decoder. The new partial product is shifted in the register and when all the bits of the second operand have been received the final product is output to a serial to parallel converter. The method and circuit permit part of the multiplication process to be performed whilst the input data is still being transmitted thereby reducing the operation delay. In a 1-bit two's complement embodiment a decoder is used to decide whether to add or subtract the received bit of the serially transmitted operand to or from the contents of the partial result register. The decoder uses knowledge of the previously transmitted bit of the operand to make this decision.

